Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. - 4.   (Cancelled.)

5. (Currently Amended)   ~~The cell search circuit of claim 3~~ A cell search circuit comprising:

a code correlator configured to correlate a received signal with a primary synchronization code;

an auxiliary code correlator having a substantially similar length as the code correlator configured to correlate the received signal with a code having a low cross correlation with the primary synchronization code; and

a scaling circuit configured to scale an output of the correlation with the primary synchronization code by an output of the auxiliary code correlator;

wherein the code having a low cross correlation with the primary synchronization code has a low cross correlation with secondary synchronization codes.

6. (Currently Amended)   ~~The cell search circuit of claim 3~~ A cell search circuit comprising:

a code correlator configured to correlate a received signal with a primary synchronization code;

an auxiliary code correlator having a substantially similar length as the code correlator configured to correlate the received signal with a code having a low cross correlation with the primary synchronization code; and

a scaling circuit configured to scale an output of the correlation with the primary synchronization code by an output of the auxiliary code correlator wherein the scaling circuit comprises a circuit performing a division function.

7. (Currently Amended) ~~The cell search circuit of claim 3 comprising~~ A cell search circuit comprising:

a code correlator configured to correlate a received signal with a primary synchronization code;

an auxiliary code correlator having a substantially similar length as the code correlator configured to correlate the received signal with a code having a low cross correlation with the primary synchronization code;

a scaling circuit configured to scale an output of the correlation with the primary synchronization code by an output of the auxiliary code correlator; and

at least one additional code correlator configured to correlate ~~for correlating~~ the received signal with a primary synchronization code, the code correlator and each at least one additional code correlator configured to process ~~processing~~ a respective set of samples corresponding to a respective multiple ~~N~~ of a chip rate of the samples.

8. (Currently Amended) The cell search circuit of claim 7 wherein the auxiliary code correlator is configured to receive only ~~receives~~ one set of the respective sets of samples.

9. (Currently Amended) A cell search circuit comprising:

a code correlator configured to correlate ~~for correlating~~ a received signal with a primary synchronization code;

an accumulator <u>configured to accumulate</u> ~~for accumulating~~ a result of the correlations of the received signal with a primary synchronization code;

a noise estimation circuit <u>configured to estimate</u> ~~for estimating~~ noise; and

a <u>computational</u> circuit <u>configured to</u> ~~for~~ functionally <u>divide</u> ~~dividing~~ the accumulated result with the estimated noise by:

determining an index of the accumulated result indicating a most significant bit;

determining an index of the estimated noise indicating a most significant bit;

subtracting the estimated noise index from the accumulated result index; and

using a result of the subtraction to determine a division of the accumulated result by the noise estimate.

10. (Currently Amended) The cell search circuit of claim 9 <u>wherein the computational circuit is</u> further ~~comprising taking~~ <u>configured to take</u> a log of n bits at and following each index in the accumulated result and the estimated noise and ~~subtracting~~ <u>to substract</u> the log of the n bits of the estimated noise from the log of the n bits of the accumulated result to determine a division of the accumulated result by the noise estimate.

11. (Currently Amended) The cell search circuit of claim 10 wherein the the <u>computational circuit is configured to take</u> ~~taking~~ a log of the n bits is by using a look-up table for n-1 bit after the index.

12. (Currently Amended) A wireless transmit/receive unit (WTRU) for performing cell search comprising:

a splitter ~~configured to receive~~ <u>receiving</u> received samples~~, and outputting~~ <u>and to output</u> a plurality of N sample sets;

N circuits receiving respective ones of the sample sets and providing respective absolute value outputs corresponding to a primary synchronization code correlation to each sample set;

N circuits providing accumulated values corresponding to the respective absolute value outputs; and

N circuits for dividing the accumulated values with an estimated noise value, and providing ratios of the accumulated values to the threshold.

13. (Currently Amended) The WRTU of claim 12 wherein ~~a value of~~ N is two and the <u>splitter is configured to output</u> ~~sample sets are an~~ even and odd sample ~~set~~ <u>sets</u>.

14. - 15.   (Cancelled)

16. (Currently Amended) ~~The WTRU of claim 14~~ <u>A wireless transmit/receive unit (WTRU) for performing cell search comprising:</u>

<u>a code correlator configured to correlate a received signal with a primary synchronization code;</u>

<u>an auxiliary code correlator having a substantially similar length as the code correlator configured to correlate the received signal with a code having a low cross correlation with the primary synchronization code; and</u>

<u>a scaling circuit configured to scale an output of the correlation with the primary synchronization code by an output of the auxiliary code correlator;</u>

wherein the code having a low cross correlation with the primary synchronization code has a low cross correlation with secondary synchronization codes.

17. (Currently Amended) ~~The WTRU of claim 14~~ <u>A wireless transmit/receive unit (WTRU) for performing cell search comprising:</u>

<u>a code correlator configured to correlate a received signal with a primary synchronization code;</u>

<u>an auxiliary code correlator having a substantially similar length as the code correlator configured to correlate the received signal with a code having a low cross correlation with the primary synchronization code; and</u>

<u>a scaling circuit configured to scale an output of the correlation with the primary synchronization code by an output of the auxiliary code correlator</u> wherein the scaling circuit comprises a circuit performing a division function.

18. (Currently Amended) ~~The WTRU of claim 14~~ <u>A wireless transmit/receive unit (WTRU) for performing cell search</u> comprising<u>:</u>

<u>a code correlator configured to correlate a received signal with a primary synchronization code;</u>

<u>an auxiliary code correlator having a substantially similar length as the code correlator configured to correlate the received signal with a code having a low cross correlation with the primary synchronization code;</u>

<u>a scaling circuit configured to scale an output of the correlation with the primary synchronization code by an output of the auxiliary code correlator; and</u>

at least one additional code correlator <u>configured to correlate</u> ~~for correlating~~ the received signal with a primary synchronization code, the code correlator and each at least one additional code correlator <u>configured to process</u> ~~processing~~ a

respective set of samples corresponding to a respective multiple N̶ of a chip rate of the samples.

19. (Currently Amended) The WTRU of claim 18 wherein the auxiliary code correlator <u>is configured to receive</u> only <s>receives</s> one set of the respective sets of samples.

20. (Currently Amended) A wireless transmit/receive unit for performing cell search comprising:

a code correlator <u>configured to correlate</u> <s>for correlating</s> a received signal with a primary synchronization code;

an accumulator <u>configured to accumulate</u> <s>for accumulating</s> a result of the correlations of the received signal with a primary synchronization code;

a noise estimation circuit <u>configured to estimate</u> <s>for estimating</s> noise; and

a <u>computational</u> circuit <u>configured to</u> <s>for</s> functionally <u>divide</u> <s>dividing</s> the accumulated result with the estimated noise by:

determining an index of the accumulated result indicating a most significant bit;

determining an index of the estimated noise indicating a most significant bit;

subtracting the estimated noise index from the accumulated result index; <u>and</u>

using a result of the subtraction to determine a division of the accumulated result by the noise estimate.

21. (Currently Amended) The WTRU of claim 20 <u>wherein the computational circuit is</u> further <s>comprising taking</s> <u>configured to take</u> a log of n bits at and following each index in the accumulated result and the estimated noise and <s>subtracting</s> <u>to substract</u> the log of the n bits of the estimated noise from the log of

the n bits of the accumulated result to determine a division of the accumulated result by the noise estimate.

22. (Currently Amended) The WTRU of claim 21 wherein the <u>computational circuit is configured to take</u> ~~taking~~ a log of the n bits is by using a look-up table for n-1 bit after the index.